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METHOD FOR FABRICATING TRANSISTORS HAVING DAMASCENE FORMED GATE CONTACTS AND SELF-ALIGNED BORDERLESS BIT LINE CONTACTS

Abstract of the Invention

A Dynamic Random Access Memory is fabricated in a semiconductor body of a first conductivity type in which there have been formed an array of memory cells which each include a trench capacitor and a vertical Insulated Gate Field Effect Transistor (IGFET). Each IGFET includes first and second output regions of a second opposite conductivity type and a gate which is separated from a surface of the semiconductor body by a gate dielectric layer. A gate electrode connected to the gate is formed using a Damascene process with insulating sidewall spacer regions being formed before the gate electrode is formed. Borderless contacts, which are self aligned, are made to the first output regions of each transistor using a Damascene process.